THAT WHICH IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate having opposing first and second surfaces, and having at least one recess extending from the second surface into interior portions;

at least one device active region formed in said semiconductor substrate adjacent the first surface thereof;

an electrical contact layer on the second surface of said semiconductor substrate; and

at least one resistivity-lowering body positioned in said at least one recess of said semiconductor substrate and connected to said electrical contact layer, said at least one resistivity-lowering body comprising a material having an electrical resistivity lower than an electrical resistivity of said semiconductor substrate to thereby lower an effective electrical resistivity thereof.

2. A semiconductor device according to Claim 1 wherein said at least one resistivity-lowering body fills an associated recess.

3. A semiconductor device according to Claim 1 further comprising a barrier layer positioned between said at least one resistivity-lowering body and the corresponding recess.

4. A semiconductor device according to Claim 1 wherein said at least one resistivity-lowering body comprises an electrical conductor having a resistivity less than about 10^{-4} Ω•cm.

5. A semiconductor device according to Claim 1 wherein said at least one recess and associated resistivity-lowering body defines a proportion of the semiconductor substrate area adjacent said at least one device active region greater than about 0.4 percent.

6. A semiconductor device according to Claim 1 wherein said at least one recess and associated resistivity-lowering body extends into said semiconductor substrate a distance greater than about 25 percent of a thickness of said semiconductor substrate.

7. A semiconductor device according to Claim 1 wherein said at least one recess and associated resistivity-lowering body comprises an array of recesses and associated resistivity-lowering bodies.

8. A semiconductor device according to Claim 7 wherein said array of recesses and associated resistivity-lowering bodies are arranged in a grid pattern.

9. A semiconductor device according to Claim 1 wherein said at least one device active region comprises at least one active region of a metal-oxide semiconductor field-effect transistor (MOSFET).

10. A semiconductor device according to Claim 9 wherein said MOSFET has a breakdown voltage of less than about 50 volts.

11. A semiconductor device according to Claim

1 wherein said at least one device active region comprises at least one active region of an insulated gate bipolar transistor (IGBT).

12. A semiconductor device according to Claim 1 wherein said at least one device active region comprises at least one active region of a microprocessor.

13. A semiconductor device according to Claim 1 wherein said substrate further comprises a relatively highly doped layer adjacent said at least one resistivity-lowering body.

14. A semiconductor device according to Claim 1 wherein said semiconductor substrate comprises silicon.

15. A semiconductor device according to Claim 14 wherein the silicon substrate has an electrical resistivity of less than about 3 mΩ•cm.

16. A semiconductor device according to Claim 1 wherein said at least one resistivity-lowering body has a thermal resistivity lower than a thermal resistivity of said semiconductor substrate.

17. A semiconductor device according to Claim 1 wherein said at least one resistivity-lowering body comprises at least one of copper, silver, aluminum, and solder.

18. A semiconductor device according to Claim 1 wherein said at least one resistivity-lowering body comprises polysilicon.

19. A semiconductor device comprising:

a semiconductor substrate having opposing first and second surfaces, and having at least one recess extending from the second surface into interior portions;

at least one metal-oxide semiconductor field-effect transistor (MOSFET) active region formed in said semiconductor substrate adjacent the first surface thereof;

a conduction terminal contact on the second surface of said semiconductor substrate; and

at least one resistivity-lowering body positioned in said at least one recess of said semiconductor substrate and connected to said conduction terminal contact, said at least one resistivity-lowering body comprising a material having an electrical resistivity lower than an electrical resistivity of said semiconductor substrate.

20. A semiconductor device according to Claim 19 wherein said at least one resistivity-lowering body fills an associated recess.

21. A semiconductor device according to Claim 19 further comprising a barrier layer positioned between said at least one resistivity-lowering body and the corresponding recess.

22. A semiconductor device according to Claim 19 wherein said at least one resistivity-lowering body comprises an electrical conductor having a resistivity less than about 10^{-4} Ω•cm.

23. A semiconductor device according to Claim 19 wherein said at least one recess and associated

resistivity-lowering body defines a proportion of the semiconductor substrate area adjacent said at least one MOSFET active region greater than about 0.4 percent.

24. A semiconductor device according to Claim 19 wherein said at least one recess and associated resistivity-lowering body extends into said semiconductor substrate a distance greater than about 25 percent of a thickness of said semiconductor substrate.

25. A semiconductor device according to Claim 19 wherein said at least one recess and associated resistivity-lowering body comprises an array of recesses and associated resistivity-lowering bodies.

26. A semiconductor device comprising:

a semiconductor substrate having opposing first and second surfaces;

at least one device active region formed in said semiconductor substrate adjacent the first surface thereof;

an electrical contact layer on the second surface of said semiconductor substrate; and

at least one resistivity-lowering body connected to said electrical contact layer and extending into interior portions of said semiconductor substrate, said at least one resistivity-lowering body comprising a material having an electrical resistivity lower than about 10^{-4} Ω•cm;

said at least one recess and associated resistivity-lowering body defining a proportion of the semiconductor substrate area adjacent said at

least one device active region greater than about 0.4 percent and extending into said semiconductor substrate a distance greater than about 25 percent of a thickness of said semiconductor substrate.

27. A semiconductor device according to Claim 26 further comprising a barrier layer positioned between said at least one resistivity-lowering body and the corresponding recess.

28. A semiconductor device according to Claim 26 wherein said at least one recess and associated resistivity-lowering body comprises an array of recesses and associated resistivity-lowering bodies.

29. A semiconductor device according to Claim 26 wherein said at least one device active region comprises at least one active region of a metal-oxide semiconductor field-effect transistor (MOSFET).

30. A semiconductor device according to Claim 26 wherein said at least one device active region comprises at least one active region of an insulated gate bipolar transistor (IGBT).

31. A semiconductor device according to Claim 26 wherein said at least one device active region comprises at least one active region of a microprocessor.

32. A semiconductor device comprising:

a semiconductor substrate having opposing first and second surfaces;

at least one device active region formed in

said semiconductor substrate adjacent the first surface thereof;

an electrical contact layer on the second surface of said semiconductor substrate; and

at least one body electrically conductive metal connected to said electrical contact layer and extending into interior portions of said semiconductor substrate, said at least one electrically conductive metal body comprising a material having an electrical resistivity lower than an electrical resistivity of said semiconductor substrate.

33. A semiconductor device according to Claim 32 wherein said at least one electrically conductive metal body comprises at least one of aluminum, copper, silver, and solder.

34. A semiconductor device according to Claim 32 wherein said at least one recess and associated electrically conductive metal body defines a proportion of the semiconductor substrate area adjacent said at least one device active region greater than about 0.4 percent.

35. A semiconductor device according to Claim 32 wherein said at least one recess and associated electrically conductive metal body extends into said semiconductor substrate a predetermined proportion of a thickness of said semiconductor substrate greater than about 25 percent.

36. A semiconductor device according to Claim 32 wherein said at least one recess and associated electrically conductive metal body comprises an array of recesses and associated bodies.

37. A semiconductor device according to Claim 32 wherein said at least one device active region comprises at least one active region of a metal-oxide semiconductor field-effect transistor (MOSFET).

38. A semiconductor device according to Claim 32 wherein said at least one device active region comprises at least one active region of an insulated gate bipolar transistor (IGBT).

39. A semiconductor device according to Claim 32 wherein said at least one device active region comprises at least one active region of a microprocessor.

40. A method for making a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity, the method comprising the steps of:

forming at least one device active region in the semiconductor substrate adjacent a first surface thereof;

forming at least one recess extending from a second surface of the substrate, opposite the first surface, into interior portions of the semiconductor substrate;

forming at least one resistivity-lowering body in the least one recess of the semiconductor substrate, the at least one resistivity-lowering body comprising a material having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate; and

forming an electrical contact layer on the second surface of the semiconductor substrate being electrically connected to the at least one

resistivity-lowering body.

41. A method according to Claim 40 wherein the step of forming the at least one resistivity-lowering body comprises filling an associated recess.

42. A method according to Claim 40 further comprising the step of forming a barrier layer lining the at least one recess.

43. A method according to Claim 40 wherein the step of forming the at least one resistivity-lowering body comprises forming same using an electrical conductor having an electrical resistivity less than about 10^{-4} Ω•cm.

44. A method according to Claim 40 wherein the steps of forming the at least one recess and associated resistivity-lowering body comprises forming same to define a proportion of the semiconductor substrate area adjacent the at least one device active region greater than about 0.4 percent.

45. A method according to Claim 40 wherein the steps of forming the at least one recess and associated resistivity-lowering body comprises forming same to extend into the semiconductor substrate a distance greater than about 25 percent of a thickness of the semiconductor substrate.

46. A method according to Claim 40 wherein the step of forming the at least one recess and associated resistivity-lowering body comprises forming an array of recesses and associated

resistivity-lowering bodies.

47. A method according to Claim 40 wherein the step of forming the array of recesses and associated resistivity-lowering bodies comprises forming same to be arranged in a grid pattern.

48. A method according to Claim 47 wherein the step of forming the grid pattern comprises cutting trenches in the second surface of said semiconductor substrate.

49. A method according to Claim 40 wherein the step of forming the at least one device active region comprises forming at least one device active region for a metal-oxide semiconductor field-effect transistor (MOSFET).

50. A method according to Claim 40 wherein the step of forming the at least one device active region comprises forming at least one device active region for an insulated gate bipolar transistor (IGBT).

51. A method according to Claim 40 wherein the step of forming the at least one device active region comprises forming at least one active region of a microprocessor.